Study of 5-Mask TFT Array Process with Low Cost, High Yield and High Performance Characteristics

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ABSTRACT

Three types of 5-mask TFT array process have been compared and analyzed their characteristics including TFT performance, process window, etc. Results showing here indicate that a 5-mask TFT manufacturing process can be optimized with low cost, high production yield and high performance. These properties let the reduced mask TFT array process reveal a much higher potential in mass production.

Keywords: 5-mask process, TFT array,

1. INTRODUCTION

Since the hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) has been considered as a good driving and switching device for the active matrix liquid crystal display (AMLCD)[1] and the other large area electronics, the TFT-LCD industry has been grown up to the mass production area. So many researches have been focused not only on the physics but also on the improvement of image quality of the large area AMLCD with low manufacturing cost and high production yield.

In order to reduce the cost and improve productivity and yield, the number of masks which are used in manufacturing process has to be reduced. It is also important that the reduction of the number of the masks has to be compromised with the improvement of performance of the TFTs and TFT-LCD panels. Typically, there are two kinds of structure in inverted-staggered TFT, back channel etched (BCE) type and etch stopper (E/S) type. Many literatures [2-8] have been proposed the ways to reduce the mask of TFT process. However, most of the proposed reduced mask TFT process only stopped in ideal level. There are many difficulties to overcome and then can reach the realistic mass production level.

In this paper, three types of 5-mask TFT manufacturing process were proposed and studied. Results showing here indicate that a 5-mask TFT manufacturing process can be optimized with low cost, high production yield and high performance.

2. PROCESS DESCRIPTIONS AND ANALYSIS

Figure 1 shows the comparison of TFT and their Cst structural cross-sections for three types 5-mask TFT manufacturing process in ERSO/ITRI. The detailed process descriptions are shown in **Figure 2(a),(b),(c)** for process A, B, C, respectively. **Figure 3** reveals the illustration of top view unit pixel, a-a' for TFT cross-section, b-b' for Cst cross-section.

Process A (**Figure 2a**) is detailed described as follow: Firstly, 200nm-thick chromium film was deposited by DC magnetron sputtering to serve as the M1 gate electrode. Next, a silicon nitride (SiNx:H) film, an intrinsic amorphous silicon (a-Si:H) film, and a P-doped amorphous silicon (n^+ a-Si:H) film were continuously deposited using PECVD apparatus. A

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busline M2 layer Cr/Al/Cr was then sputtered immediately. The -thickness of SiNx:H, a-Si:H, n^+ a-Si:H and Cr/Al/Cr are 370nm, 150nm, 30nm and 50/600/100nm, respectively. And the RF power densities for SiNx:H, a-Si:H and n^+ a-Si:H are 120, 10 and 20 mW/cm^2, respectively. During the PECVD process, substrate temperature was kept at 280°C. The source-drain and busline metals Cr/Al/Cr layers were patterned. Then the n+ a-Si:H and a-Si:H layers were in both TFT and Cst area.

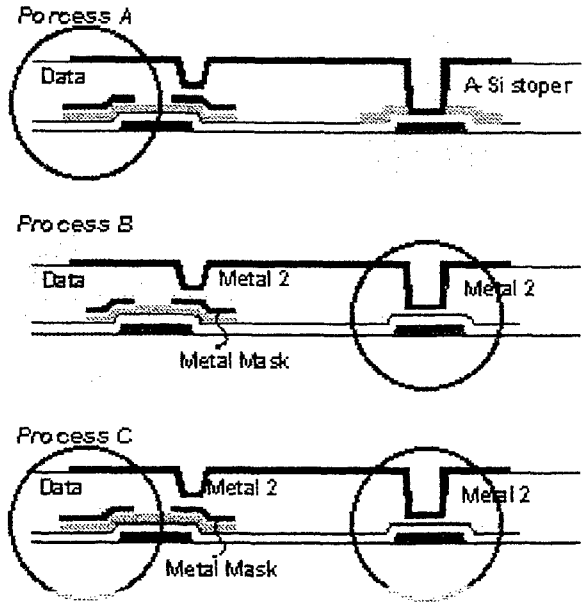


Figure 1. The comparison of three types of 5-mask TFT manufacturing process.

The purpose of Cst a-Si layer is to be an etching stopper. It is in order to avoid the etching through the gate SiNx and damaging the Cst in the next etching process. If it uses the metal as the etching stopper, the Cst structure will be the metal/n+a-Si:H/a-Si:H/SiNx/metal. It is hard to control the variation of storage capacitance when the gate pulse driving in the Cs on gate mode. After the n+ a-Si:H channel etched, the passivation layer was then deposited and patterned. The pattern areas locate not only in the TFT 's source area for pixel electrode conducting, but also in the Cst area for ITO/gate SiNx/M1 structure. Accordingly, a complicated etching recipe was needed for high selectivity for passivation materials to a-Si:H and then a recipe with high selectivity of a-Si:H to gate SiNx. Finally, the pixel electrode was then sputtered and patterned for top-ITO structure to finish the TFT process.

It was found there are some advantages in this process. (1) Mask numbers wer reduced to 5; (2) Buslines, source-drain metal (M2) layer was the 2nd mask. It could improve significantly the open-line defects issue due to the reduction of particles coming from the photolithography process when compare to the conventional process. (3) Continuously sputtered the metal after PECVD deposition of active layers gate SiNx, a-Si:H and n+a-Si:H. It can improve the source-drain metal to n+a-Si:H contact resistance.[9] In the conventional process, the TFT is usually dipped in BOE solution before drain metal sputtering to exclude the native oxide on the n+ a-Si:H surface and thus ensure a good contact between n+a-Si:H and the drain metal. However, the interface of n+a-Si:H/drain metal is hardly well controlled due to the limitation of BOE solution. (4) It don't need island taper for M2 to island step coverage due to the M2/island stack structure (no step coverage in M2/island). Hence,

the open-line defects probability also can be lowered. However, there are some drawbacks, including: (1) It needs complicated etching process in making Cst structure. (2) The storage capacitance of Cst area completely depends on the area of passvation etching hole. It will reduce the aperture ratio due to enlarge the M1 area for keeping the same capacitance value.

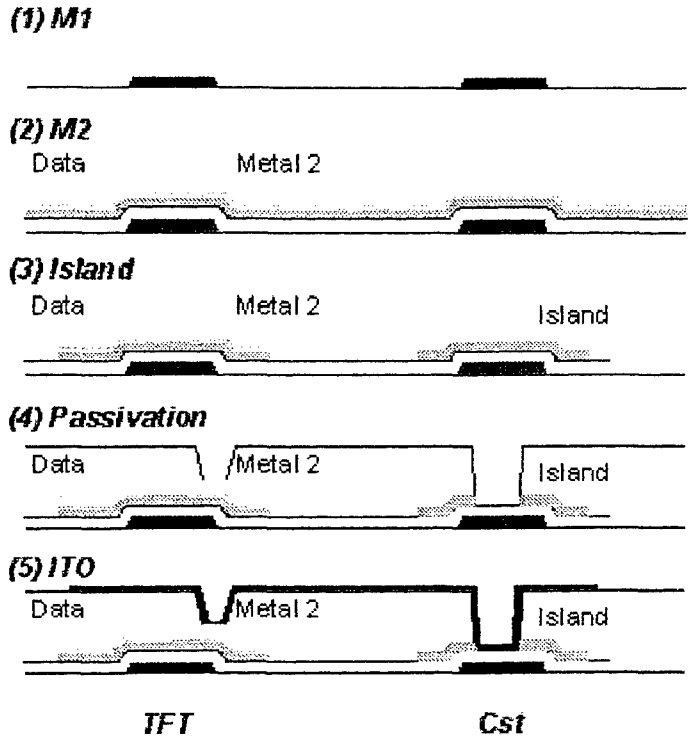


Figure 2a. The process flow of ***Process A***

Process B possesses an island metal masking structure [10] is shown in **Figure 2b**. This process can be compromised with the same mask in Process A and accomplished in rearrangement of the process sequence: M1, I/metal making, M2, Passivation, and ITO.

In this process, the protected channel metal was etched in S/D metal mask patterning simultaneously. This metal masking structure will serve an extra advantage, e.g., the plasma damage free in the dry etching or oxygen ashing process. It also provides a same S/D metal to n+a-Si:H contact resistance like Process A. Accordingly, the TFT performance will be good as Process A. Moreover, Process B will give a wider process window of controlling TFT characteristics than Process A due to the prevention of plasma damage On the other hand, the different process sequence of M2 and I will provide a better Cst structure: metal/gate SiNx/metal than Process B (see **Figure 1**). Unfortunately, although it can solve the drawbacks of Cst problems and possess the same TFT performance of Process A, it can not avoid the M2 to metal masking/island high step coverage. This phenomenon will seriously cause the increasing of buslines open-line defects.

From the discussion mentioned above, it can be seen the comparison of two types of Process A and Process B in **Figure 1**. How to get the all advantages of two processes? A total solution is shown in Process C.

The process C sequence follows the Process B as M1, I/metal masking, M2, Passivation, ITO to solve the Cst process issue and keep the excellent TFT performance. But it needs a modification in I/metal masking layout to achieve the M2 open-line defect free like the Process A type's advantage in TFT and M2. The concept is presented in **Figure 4**. The final Process C could possess not only an excellent TFT quality (from better S/D metal contact resistance) and uniformity (from reduction of plasma damage in TFT). Moreover this process could possess a better Cst structure (metal/SiNx/metal) for etching process window and driving capability. On the other hand, it also provides a good process window for busline open-line defects controlling (due to two times of metal sputtering in island metal masking structure and M2, see **Figure 4**). This property will be much better than the M2 process in Process A. It is believed that the process C will be a low cost, high yield and high performance properties good process in mass production.

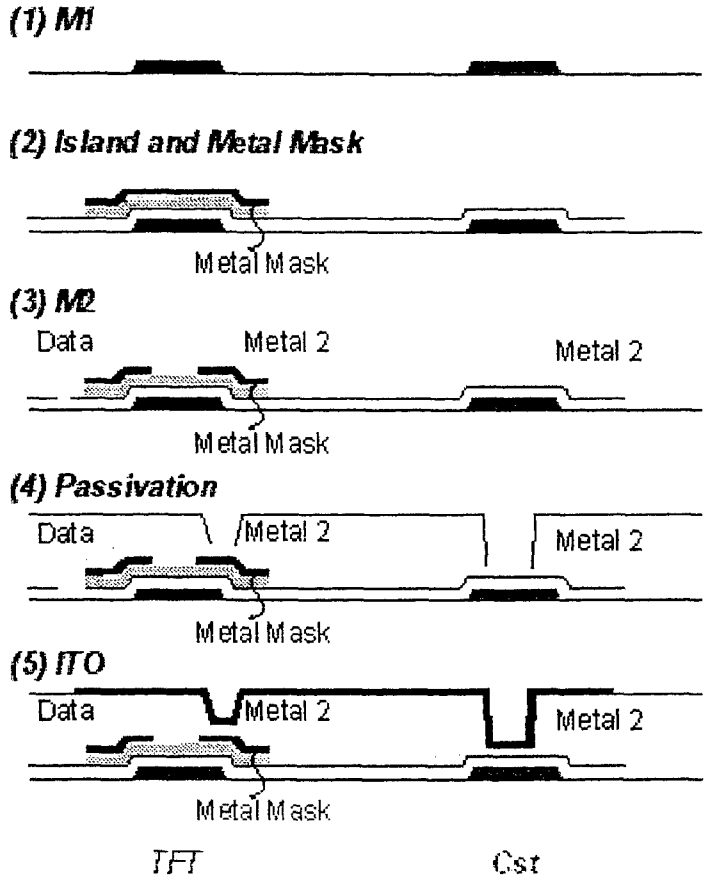


Figure 2b. The process flow of ***Process B***

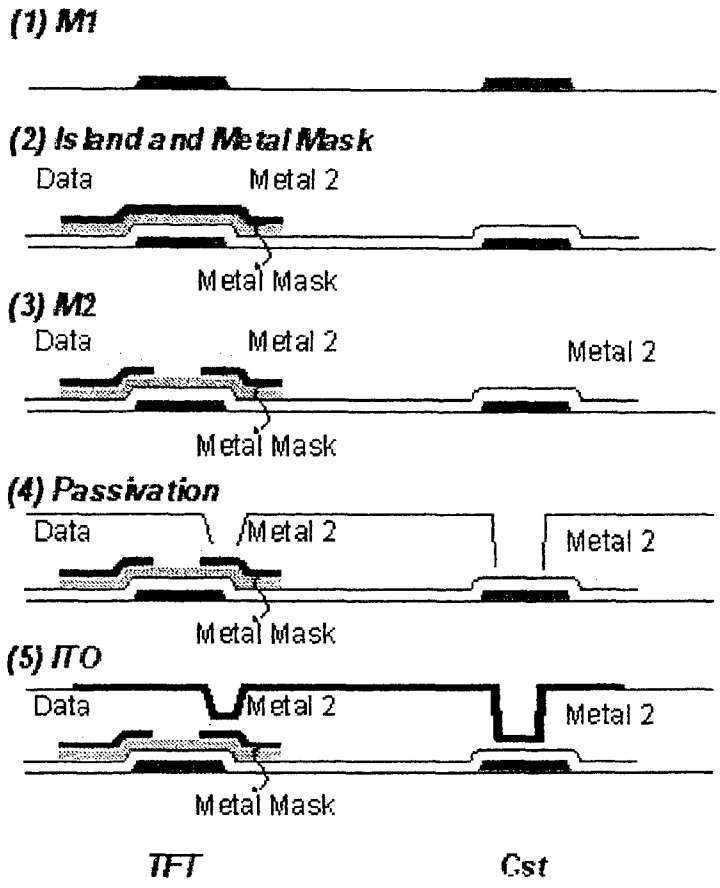


Figure 2c. The process flow of *Process C*

3. CONCLUSION

In this paper, three types of 5-mask TFT array process have been compared and analyzed their characteristics. These characteristics include TFT structure, performance, and process window, etc. Results showed here indicate that a 5-mask TFT manufacturing process (process C) can be optimized with low cost, high production yield and high performance. These properties let the reduced mask TFT array process (process C) reveal a much higher potential in mass production.

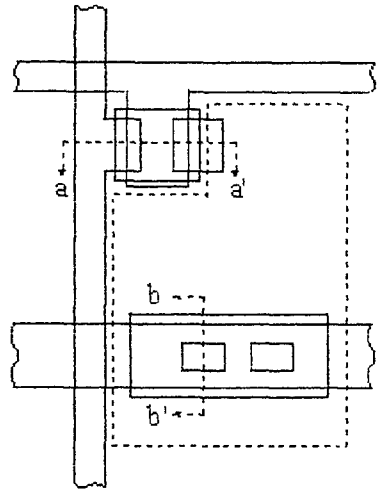
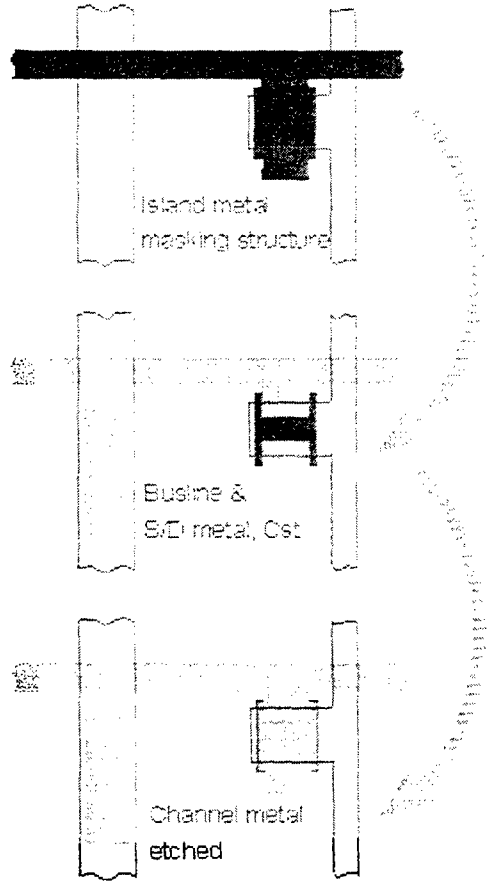


Figure 3. The illustrated top view unit pixel, a-a' for TFT cross-section, b-b' for Cst cross-section, related to Figure 1 and Figure 2.



Figrue 4. The Process C layout illustration

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